WHAT IS CLAIMED IS:

1. An integrated circuit comprising:

an active termination circuit having first and second transistors of opposite type coupled in series between a Vdd node of a first source potential and a Vss node of a second source potential, the second source potential being lower than the first source potential, the at least one termination node being coupled to a common node between the first and second transistors; and

a control circuit operable to bias the first and second transistors.

2. The integrated circuit as in claim 1 wherein the control circuit is operable to bias the first and second transistors such that they provide a clamping function at the common node.

3. The integrated circuit of claim 1 wherein the first transistor is a MOSFET of the N-channel type and the second transistor is a MOSFET of the P-channel type;

the drain of the first MOSFET is coupled to the Vdd node, and the drain of the second MOSFET is coupled to the Vss node; and

the sources of both MOSFETs are coupled together and to the common node.

4. The integrated circuit of claim 1 wherein:

the control circuit includes a first control terminal control circuit operable to provide a first control terminal drive signal to a control terminal of the first transistor, and a second control terminal control circuit operable to provide a second control terminal drive signal to a control terminal of the second transistor; and

the first and second control terminal drive signals are such that a quiescent voltage potential of the common node is between the Vdd and Vss potentials.

5. The integrated circuit of claim 4 wherein the quiescent voltage potential of the common node is at about a midpoint between the Vdd and Vss potentials.

6. The integrated circuit of claim 4 wherein the first and second control terminal control circuits are operable to provide a first control terminal drive signal to a control terminal of the first transistor and a second control terminal drive signal to a control terminal of the second transistor to control the quiescent switch current through the first and second transistors.

7. The integrated circuit of claim 4 wherein the first control terminal drive signal to a control terminal of the first transistor and the second control terminal drive signal to a control terminal of the second transistor are preferably controlled such that the quiescent current conducted through the switch is substantially less than the current through two resistors whose parallel resistance approximates the characteristic impedance of a coupled transmission line.

8. The integrated circuit of claim 4 wherein the device geometries, device size, and processing of the first and second transistors are scaled so that they achieve a controlled impedance and a quiescent voltage potential at the common node in response to an induced voltages produced by the driver circuit coupling communication signals to the termination node, and the quiescent voltage potential is at about a midpoint between the Vdd and Vss potentials.

9. The integrated circuit of claim 4 wherein the first and second control terminal control circuits are operable from voltage sources that are greater than the source potential Vdd for the first control terminal control circuit, and less than the source potential Vss for the second

control terminal control circuit, and are capable of providing control terminal control signals, respectively, that are greater than the source potential Vdd and less than the source potential Vss.

10. The integrated circuit of claim 1 and further comprising:

a third transistor having a current path and a control terminal, the current path coupled between the first transistor and the voltage source Vdd; and

a fourth transistor, having a current path and a control terminal, the current path coupled between the second transistor and the voltage source Vss wherein the operation of the first and second transistors can be selectively enabled or disabled by control signals coupled to the control terminals of the third and fourth transistors.

11. The integrated circuit of claim 10 wherein the third transistor is a P-channel MOSFET and the fourth transistor is an N-channel MOSFET.

12. The integrated circuit of claim 1 wherein the control terminal control circuit preferably includes a fifth transistor and a sixth transistor in series across a Vdd node of a first source potential and a Vss node of a second source potential and scaled to the first and second transistors; and

a current source coupled to at least one of the fifth or sixth transistor that controls the quiescent current level in the first and second transistors.

13. The integrated circuit of claim 12 wherein the fifth transistor is an N-channel MOSFET, and the sixth transistor is a P-channel MOSFET.

14. The integrated circuit of claim 1 wherein the control circuit preferably includes a voltage source operable to produce a voltage potential of about a midpoint of the voltages of the voltage sources Vdd and Vss.

15. The integrated circuit of claim 1 wherein the control circuit preferably includes a voltage source operable to produce a voltage potential responsive to an externally supplied input voltage.

16. The integrated circuit of claim 1 and further comprising a resistor coupled between the common node and the termination node.

17. An active termination circuit, comprising:

a first MOSFET having a gate terminal, a drain terminal, and a source terminal, the source terminal coupled to a common node, and the drain terminal coupled to a Vdd node of a first source potential;

a second MOSFET having a gate terminal, a drain terminal, and a source terminal, the source terminal coupled to the common node, and the drain terminal coupled to a Vss node of a second source potential, the second source potential being lower than the first source potential; and

a control circuit operable to bias the first and second MOSFETs.

18. The active termination circuit of claim 17 wherein the control circuit operates to bias the first and second MOSFETs such that they exhibit a controlled impedance at the common node.

19. The active termination circuit of claim 17, wherein the first MOSFET is an N-channel MOSFET and the second MOSFET is a P-channel MOSFET.

20. The active termination circuit of claim 17, wherein the gate of the first MOSFET is coupled to a voltage source between the Vdd and Vss potentials and the gate of the second MOSFET is coupled to another voltage source of a lower potential.

21. The active termination circuit of claim 20, wherein the potential difference between the voltage sources coupled to the gates of the first and second MOSFETs is controlled by a current source.

22. The active termination circuit of claim 17 wherein the control circuit comprises:

a first operational amplifier with an output coupled to the gate terminal of the first MOSFET; and

a second operation amplifier with an output coupled to the gate terminal of the second MOSFET.

23. The active termination circuit of claim 22 wherein the first MOSFET is an N-channel MOSFET and the second MOSFET is a P-channel MOSFET and wherein the first operational amplifier is powered by a power supply potential greater than Vdd and the second operational amplifier is powered by a power supply potential less than Vss, the first and second operational amplifiers capable of producing gate drive signals greater than the power supply potential Vdd and less than the power supply potential Vss, respectively.

24. The active termination circuit of claim 23 and further comprising:

a third MOSFET with a channel coupled between Vdd and the first operational amplifier, the third MOSFET having a gate terminal coupled to the gate terminal of the first MOSFET, the third MOSFET being an N-channel MOSFET; and

a fourth MOSFET with a channel coupled between Vss and the first operational amplifier, the fourth MOSFET having a gate terminal coupled to the gate terminal of the second MOSFET, the fourth MOSFET being a P-channel MOSFET.

25. The active termination circuit of claim 17 and further comprising a first enable switch coupled between the first MOSFET and Vdd and a second enable switch coupled between the second MOSFET and Vss.

26. An active termination circuit, comprising:

a first bipolar transistor having a base terminal, a collector terminal, and an emitter terminal, the emitter terminal coupled to a common node, and the collector terminal coupled to a Vdd node of a first source potential;

a second bipolar transistor having a base terminal, a collector terminal, and a emitter terminal, the emitter terminal coupled to the common node, and the emitter terminal coupled to a Vss node of a second source potential, the second source potential being lower than the first source potential; and

a control circuit operable to bias the first and second bipolar transistors such that they exhibit a controlled impedance at the common node.

27. A method of operating an active termination circuit, the method comprising:

biasing first and second series coupled transistors of opposite type such that they exhibit a controlled impedance at a common node thereof, wherein the first and second transistors are coupled in series across a Vdd node of a first source potential and a Vss node of a second source potential, the common node being between the first and second transistors , and the second source potential being lower than the first source potential.

28. The method of claim 27 wherein biasing first and second series coupled transistors comprises producing first and second control terminal drive signals and applying said first and second control terminal drive signal to the first and second series coupled transistors, the first and second control terminal drive signals produced such that a quiescent voltage potential of the common node is between the Vdd and Vss potentials.

29. The method of claim 28 wherein the first and second series coupled transistors are MOSFETs.

30. The method of claim 27 wherein the quiescent voltage potential of the common node is produced at about a midpoint between the Vdd and Vss potentials.

31. The method of claim 27 and further comprising scaling device geometries, device size, and processing of the first and second MOSFETs so that their coupled sources produce a controlled impedance and a quiescent voltage potential at the common node in response to an induced voltages produced by the driver circuit coupling communication signals to the termination node.